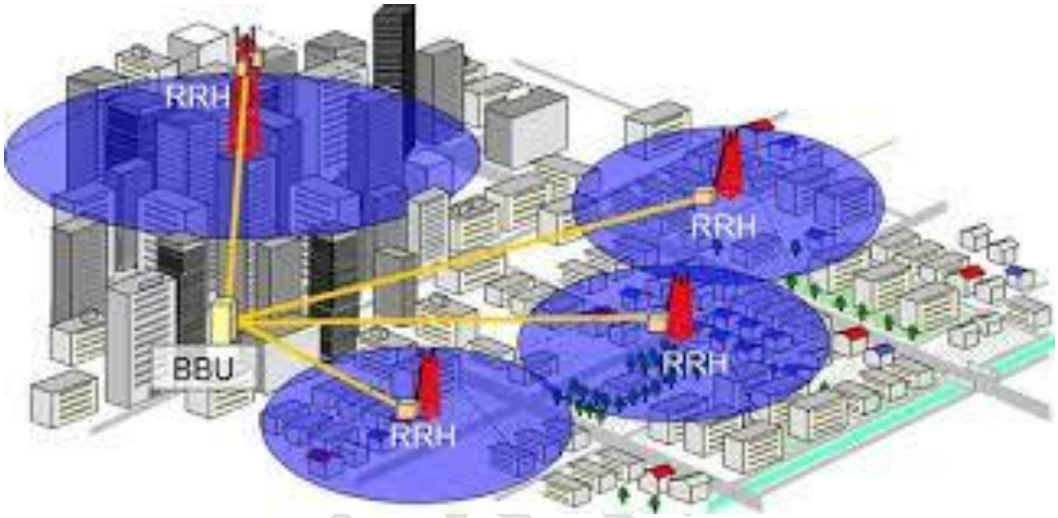
Orion IPL8101TX - CPRI over OTN Processor Core

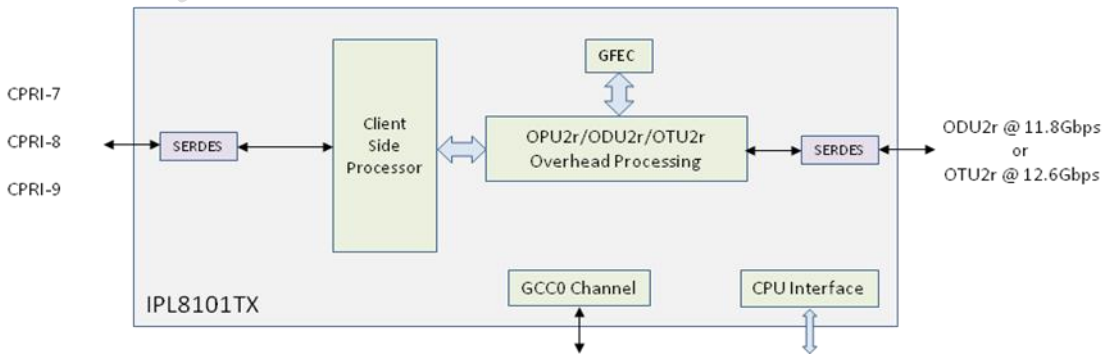
An IP Core OTN processor optimized for Cloud-RAN (C-RAN)
Mobile Front-Haul (MFH) applications.

C-RAN Architecture:



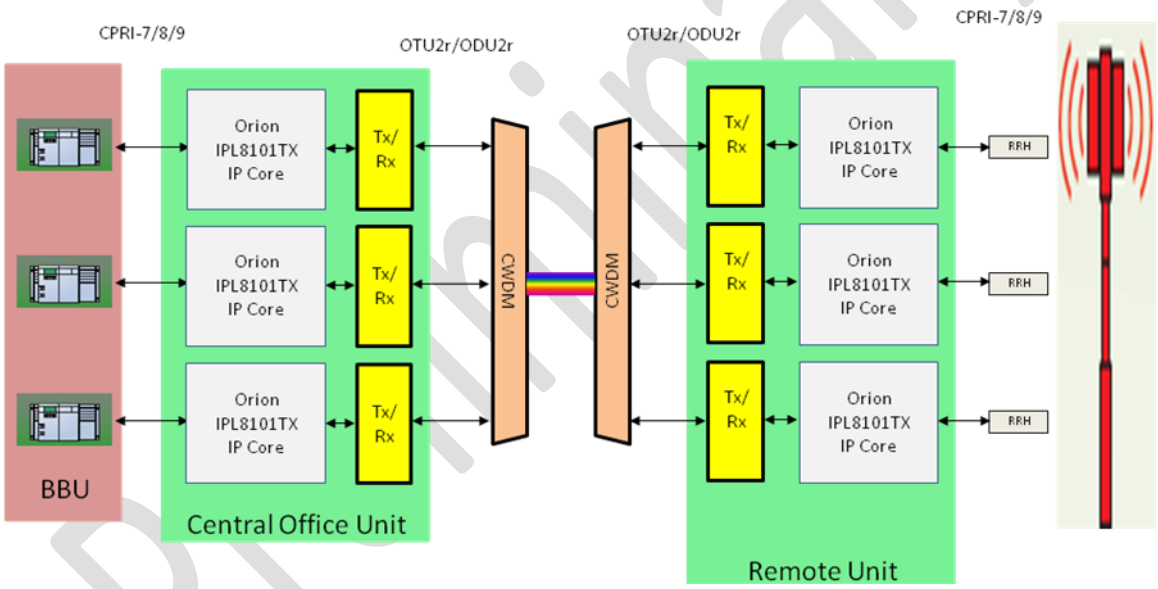
The ORION IPL8101TX incorporates a mapping scheme for CPRI signals which optimizes the transport of CPRI (Common Public Radio Interface) signals between RRH (Remote Radio Head) antennas and centralized BBU (Base Band Unit) sites. It includes optional Forward Error Correction (FEC) and supports CPRI signals Option 7, Option 8 and Option 9.

IPL8101TX CPRI over OTN Processor IP Core Block Diagram



IP Light's Orion CPRI over OTN Processors have been optimized for the effective transport of CPRI signals over fiber networks between RRH and BBU sites. The IPL8101TX Processor synchronously maps the CPRI data into an OPU2r container and presents the signal to the line port as 12.6Gbps OTU2r signal or 11.8Gbps ODU2r (OTU2r No FEC) signal.

Typical Application: 3 x CPRI-7/8/9



IPL8101TX CPRI over OTN Processor IP Core: Key Features and Benefits

Line Ports: • OTU2r (12.639Gbps) • ODU2r (11.846Gbps) • Integrated GFEC • G.709 performance Monitoring and Alarms	Extremely low latency: • Less than 0.7 µSec End-to-End CPRI signal delay • Less than 6µSec End-to-End CPRI signal delay with GFEC.	• Meets CPRI Specification V6.1 requirements • Jitter/Wander control by flexible timing methods
Client Ports: • CPRI option 7 (9.830Gbps) • CPRI option 8 (10.137Gbps) • CPRI option 9 (12.165Gbps) • PCS Monitoring and Alarms		• Alarm supervision, suite of maintenance capabilities. • Register based Configuration and Control • Easy and Simple integration into Xilinx's Kintex UltraScale FPGA family
Xilinx FPGA Utilization: • **75,000 flip-flops** • **80,000 LUTs** • **200,000 memory bits** • **2 transceivers (GTH), operating speed up to 12.65Gbps**		